Certificate
AUG 15 2005
of Correction

TRANSMITTAL FORM

(to be used for all correspondence during pendency of filed application)

Patent Number	6,886,153 B1
Issue Date	April 26, 2005
First Named Inventor	Christopher F. Bevis
Serial Number	10/029,521
Filing Date	December 21, 2001
Total Number of Pages in This Submission: 16	Attorney Docket Number: 22120-06499

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form (in duplicate)
  - ☐ Check Enclosed
- ☒ Return Receipt Postcard
- ☐ Response to Notice to File Missing Parts
- ☐ Assignment & Recordation Cover Sheet
- ☐ Declaration
- ☐ Power of Attorney
- ☐ Application Data Sheet
- ☐ Information Disclosure Statement & PTO/SB/08A
  - ☐ Copies of IDS Cited References
- ☐ Request for Corrected Filing Receipt
- ☐ Request for Correction of Recorded Assignment
- ☐ Amendment/Response: [ ] Page(s)
  - ☐ After Final
- ☐ Status Request
- ☐ Revocation and Substitute Power of Attorney
- ☐ Issue Fee Transmittal
- ☐ Letter to Chief Draftsperson
- ☐ Formal Drawing(s):
  - [ ] Sheet(s) of Figure(s) [ ]
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Certified Copy of Priority Document(s)
- ☐ After Allowance Communication to Group
- ☒ Request for Certificate of Correction
- ☒ Form PTO-1050 (in duplicate)
- ☒ Copy of Amendment Filed September 23, 2004
- ☐ _____
- ☐ _____
- ☐ _____

REMARKS:

SIGNATURE OF ATTORNEY OR AGENT

Signature:			
Attorney/Reg. No.:	**Rimma Budnitskaya, Reg. No. 48,237**	Dated:	8/2/05

CERTIFICATE OF MAILING

I hereby certify that this correspondence, including the enclosures identified above, is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below. If the Express Mail Mailing Number is filled in below, then this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service pursuant to 37 CFR 1.10.

Signature:			
Typed or Printed Name:	**Rimma Budnitskaya**	Dated:	8/2/05
Express Mail Mailing Number *(optional)*:			

IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

APPLICANTS:	Christopher F. Bevis
PATENT NO.:	6,886,153 B1
ISSUE DATE:	April 26, 2005
SERIAL NO.:	10/029,521
FILING DATE:	December 21, 2001
TITLE:	Design Driven Inspection or Measurement for Semiconductor Using Recipe
ATTY. DKT. NO.:	22120-06499

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below:

Dated: 8/2/05 By: _____
Rimma Budnitskaya, Reg. No. 48,237

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

ATTENTION: DECISION AND CERTIFICATE OF CORRECTION
BRANCH OF THE PATENT ISSUE DIVISION

REQUEST FOR CERTIFICATE OF CORRECTION

SIR:

The following error, as more fully described below, appear in this patent.

☒ The Applicant submits that no fee is due for correction of the error made by the Patent and Trademark Office; OR,

☐ The errors occurred in good faith. Correction thereof does not involve such changes in the patent as would constitute new matter or would require re-examination. A Certificate of Correction is requested. Enclosed herewith is payment in the amount of $100.00 to cover the fee for this Certificate of Correction.

Attached hereto are duplicate Forms PTO-1050, with at least one copy that is suitable for printing. Also enclosed is a copy of an Amendment filed on September 23, 2004 showing the text of the allowed claims.

Applicant kindly requests the following change:

Claim 3, at column 12, line 37, please change "comprises" to "comprise".

Please send the Certificate to:

RIMMA BUDNITSKAYA
Fenwick & West LLP
Silicon Valley Center
801 California Street
Mountain View, CA 94041

Respectfully submitted,
CHRISTOPHER F. BEVIS

Dated: August 2, 2005

By: _____

RIMMA BUDNITSKAYA, REG. NO. 48,237
FENWICK & WEST LLP
Silicon Valley Center
801 California Street
Mountain View, CA 94041
Tel.: (415) 875-2401
Fax.: (415) 281-1350

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,886,153 B1

DATED: April 26, 2005

INVENTORS: Christopher F. Bevis

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 3, at column 12, line 37, please change "comprises" to "comprise.

MAILING ADDRESS OF SENDER:
Rimma Budnitskaya
Fenwick & West LLP
275 Battery Street
San Francisco, CA 94111

PATENT NO. 6,886,153 B1

No, of add'l copies
@50¢ per page
⇨ _____

AUG 15 2005

22120/06499/SF/5148514.1

IN THE

UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Christopher F. Bevis
SERIAL NO.:	10/029,521
FILING DATE:	December 21, 2001
TITLE:	Inspection of Semiconductor Devices Using Design Data
EXAMINER:	Thuan V. Do
GROUP ART UNIT:	2825
ATTY. DKT. NO.:	22120-06499

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Dated: September 23, 2004 By: _____

Rimma Budnitskaya, Reg. No. 48,237

MAIL STOP AMENDMENT
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111

Sir:

This amendment for the patent application identified above is in response to the Office Action dated June 24, 2004, which set a shortened statutory period for response that expires on September 24, 2004.

Amendments to Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 7 of this paper.

Kindly amend this application as follows.

AMENDMENTS TO THE SPECIFICATION

Please amend the Title as follows:

"~~Design Driven Inspection of Measurement~~" to "Inspection of Semiconductor Devices Using Design Data."

CLAIM AMENDMENTS

Please amend claims 1-3, 17, and 23 as indicated below.

1. (Currently Amended) For an instrument responsive to recipe parameters, a method for creating a recipe, the method comprising:

accessing mask set data;

recognizing a target structure in the mask set data;

extracting parameters from the mask set data; and

configuring the recipe based on the extracted parameters responsive to the recognized target structure, wherein the ~~configuring~~ configuration of the recipe is performed before a wafer printed with a mask created from the mask set data is generated.

2. (Currently Amended) The method of claim 1 wherein the ~~recipe~~ parameters for a process layer ~~is~~ are queried from a database.

3. (Currently Amended) The method of claim 1 wherein the ~~recipe~~ extracted parameters comprises at least one of wafer processing parameters, inspection parameters, and control parameters.

4. (Original) The method of claim 1 wherein the target structure comprises at least one of alignment site, measurement site, overlay target, and array element.

5. (Previously Presented) For an instrument instructed by a recipe to perform a task on a wafer, a method comprising:

receiving design data describing a die;

extracting parameters from the design data relevant to the configuration of the instrument;

and

creating from the extracted parameters, the recipe for performing the task, wherein the recipe is created before a wafer to which the design data has been applied is generated.

6. (Original) The method of claim 5 wherein the task includes at least one of inspection and metrology.

7. (Previously Presented) The method of claim 5 further comprising applying the extracted parameters to at least one die on the wafer using a stepper setup file.

8. (Original) The method of claim 5 wherein the design data includes at least one of element names and instance types.

9. (Original) The method of claim 5 further comprising inspecting the wafer using the recipe.

10. (Original) The method of claim 9 wherein the inspecting is micro inspection.

11. (Original) The method of claim 9 wherein the inspecting is macro inspection.

12. (Original) The method of claim 9 wherein the inspecting is darkfield inspection.

13. (Original) The method of claim 5 further comprising measuring the wafer using the recipe.

14. (Original) The method of claim 13 wherein the measuring is film measurement.

15. (Original) The method of claim 13 wherein the measuring is critical dimension measurement.

16. (Original) The method of claim 13 wherein the measuring is overlay measurement.

17. (Currently Amended) A recipe extraction system using design data specifying one or more die, the system comprising:

an access module to access the design data describing a die;

an analyzer to extract parameters from the design data; and

a configuration module to produce a recipe for controlling one of an inspection and a metrology instrument, wherein the configuration module produces the recipe before a wafer to which the design data has been applied is generated.

18. (Original) The system of claim 17 wherein the access module is a network interface.

19. (Original) The system of claim 17 wherein the analyzer performs overlay recipe extraction.

20. (Original) The system of claim 17 wherein the analyzer performs inspection recipe extraction.

21. (Original) The system of claim 17 wherein the recipe is a set of instructions for measuring a wafer.

22. (Original) The system of claim 17 wherein the recipe is a set of instructions for inspecting a wafer.

23. (Currently Amended) An inspection/metrology instrument using design data specifying one or more die, the instrument comprising:

an input interface for accessing the design data describing a die;

an analyzer to recognize target structures in the design data and extract parameters from the design data; and

a recipe module creating a recipe based on the extracted parameters responsive to the

recognized target structure, wherein the recipe module creates the recipe before a wafer to which the design data has been applied is generated.

24. (Cancelled).

25. (Cancelled).

26. (Cancelled).

27. (Cancelled).

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

Nara does not disclose or suggest the claimed invention. Although Nara is directed to a system and method for setting up a recipe on an inspection tool, the configuration of the recipe is performed in a completely different manner than in the claimed invention. The inspection tools in Nara require the existence of a wafer for a given device type and layout in order to generate a recipe, thereby introducing an undesirable time lag between the time a wafer is available for a given device and a first measurement or inspection can be performed. Additionally, the method of Nara requires a skilled operator to be present to generate the recipe.

Examiner asserts in his rejection that Nara discloses "accessing mask set data" at col. 1, lines 25-30. Neither the cited passage of the reference nor the rest of the disclosure, however, disclose the claimed invention. Rather, the cited passage discloses a conventional method of manufacturing a semiconductor device by transferring a circuit pattern formed on a photomask to a semiconductor wafer by a lithographing process (Nara, col. 1, lines 25-32). The word "photomask" is used by Nara to describe conventional manufacturing process of a semiconductor device. Nara is not even concerned with accessing mask set data to generate a recipe for inspection of a semiconductor device because Nara requires existence of a wafer to generate a recipe.

Similarly, Nara does not disclose or suggest the step of "extracting parameters from the mask set data." Examiner asserts in his rejection that this step is disclosed at col. 4, lines 57-67 of Nara. Instead, the cited portions of the reference disclose:

> "...an image from an external apparatus can be displayed on the monitor of the inspection apparatus for **extracting a defect** of the inspection-subject substrate." (Emphasis added).

The cited paragraph explicitly requires the use of an image derived from observing the wafer with an imaging tool such as an optical or electron beam inspection tool. "Extracting

parameters from the mask set data," as claimed, is different from "extracting a defect of the inspection-subject substrate," as disclosed in Nara, since the mask set data from which the parameters are extracted is generated before a wafer printed with a mask created from the mask set data is generated. In contrast, in Nara, a defect is extracted from a specific wafer that is in existence when the defect is extracted.

Moreover, Nara does not disclose or suggest the recipe configuration step. Examiner cites col. 32, lines 55-65 of Nara for a disclosure of this claimed feature. The cited passage of the reference describes a diagram shown in Fig. 29 of the picture plane in the inspecting mode. As shown in Fig. 29 of Nara, region 909 displays "inspection progress" and "the number of defects." This requires the existence of a wafer. Region 908 of Fig. 29 explicitly references the location of the wafer ("Shelf Number B15) and identity code for the specific wafer ("Wafer ID22 Lot ID 11"), thereby explicitly requiring the existence of the wafer. Similarly, at col. 16, lines 19-58 Nara describes a recipe forming procedure that requires that a wafer be in existence to generate a recipe. By contrast, in the claimed invention, the configuration of the recipe is performed before a wafer printed with a mask created from the mask set data is generated.

For at least the reasons discussed above, independent claims 1, 5, 17, and 23 patentably distinguish over the cited references. Dependent claims 2-4, 6-16, and 18-22 variously depend from claims 1, 5, 17, and 23 and are patentably distinct for at least the reasons cited above in addition to reciting their own patentable features.

For example, claim 3 further recites "wherein the extracted parameters comprise at least one of wafer processing parameters, inspection parameters, and control parameters." Claim 3 is not disclosed or suggested by Nara. Col. 4, lines 30-40 of Nara cited by the Examiner to support the rejection of claim 3 disclose a user interface display in which parameters are being inputted

by a human operator of the instrument. In contrast, the parameters recited in claim 3 are extracted from the mask set data rather than being manually inputted by a human operator.

Conclusion

In sum, Applicant respectfully submits that claims 1-23, as presented herein, are patentably distinguishable over the cited reference (including references cited, but not applied). Therefore, Applicant requests reconsideration and allowance of these claims.

RESPECTFULLY SUBMITTED,
Christopher F. Bevis

Date: September 23, 2004 By: _____

Rimma Budnitskaya, Reg. No. 48,237
FENWICK & WEST LLP
Silicon Valley Center
801 California Street
Mountain View, CA 94041
Phone: (415) 875-2401
Fax: (415) 281-1350